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Back channel etch chemistry of advanced a-Si:H TFTs

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ABSTRACT

We report on the effects of back channel etch depth and etchant chemistry on the electrical characteristics of inverted staggered advanced amorphous silicon thin-film transistors. We found that the optimum amorphous silicon film thickness in the channel is about 800–1100 Å. Three dry etch, HBr + Cl_2, C_2F_6, and $CCl_2F_2 + O_2$, and one wet etch, KOH, chemistries are used for the back channel etch processing. We established that dry etch can be used for the back channel etch of amorphous silicon transistor without degrading its electrical characteristics.

1. Introduction

Hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) technology can be found in a variety of electronic applications ranging from flat panel displays [1–4] to sensors [5–8]. A transistor's electrical performance is intimately related to its fabrication processes, especially during dry etching steps where the device is exposed to high energy radiation and ions [9,10]. For the a-Si:H TFT with inverted staggered back channel etch (BCE) type structure, an etching of the channel region amorphous silicon film is required after the source and drain definition to reduce its off-current (I_{OFF}) [11]. This BCE process is a critical step, because the plasma generated during the reactive ion etching (RIE) can degrade the TFT's field-effect mobility (μ_{EFF}) by up to 15% compared to the same TFT etched with wet etchant [12]. Even though the a-Si:H TFT can be fabricated completely using wet etch process only [13], dry etch is still the preferred method for critical etching steps due to its superior selectivity versus metal and photoresist (PR), high anisotropy, and reduced residue formation [14]. Thus it would be desirable to search for a dry etchant that encompasses the benefits mentioned above regarding dry etching without degrading the electrical properties of the transistor.

Numerous dry and wet etchants have been reported in the etching of silicon for various applications [15,16]. Fluorocarbon compounds, such as C_2F_6 and CF_4, have been used as RIE gas species to etch the n^+ (phosphorous-doped) amorphous silicon [17]. Alternatively, chlorofluorocarbon compounds like CCl_2F_2 and CF_3Cl have also been utilized to dry etch the n^+a-Si:H due of its high selectivity versus intrinsic a-Si:H; they also do not leave organic etching by-product common in fluorocarbon dry etching process [18,19]. Hydrogen bromide (HBr) has often been used to dry etch silicon-based devices because of its high selectivity versus oxide, and high aspect ratio of the profile [19]. For plasma-free etching of the silicon film, potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH) have been employed [20,21]. With such a diverse range of BCE etchants, a comprehensive study of their impacts on the electrical performance of the a-Si:H TFT is needed in order to select, if any, the best dry etchant chemistry for the back channel etch fabrication process.

Choe and Kim evaluated the effect of dry etchants on the off-current of the amorphous silicon thin-film transistors, and related the increase in off-current to the increase in contaminant ($MoCl_X$ and MoF_X) concentrations in the TFT's back channel [22]. GadelRab et al. compared the difference in TFT electrical performance between tri-layer transistors etched with SF_4:O_2 plasma, and KOH [9], and concluded that the wet etched device shows higher electrical performance. Additionally, Ando et al. presented an in-depth analysis regarding the effect of back channel etching depth and etchants (i.e. fluorine-based gas and hydrazine monohydrate) on the TFT electrical characteristics, and concluded that dry etching degrades the field-effect mobility of the a-Si:H TFT [12]. With our best effort, however, we cannot find a published study that assesses the influence of a wide array of back channel etchants, with distinct etching chemistries and mechanisms, on the electrical performance of the advanced a-Si:H TFT's [23]. The advanced a-Si:H TFT is a transistor with a multi-layer structure in the gate dielectric and channel region. In this device, both the gate insulator and the active material are deposited with different process rates using a

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two-step plasma enhanced chemical vapor deposition (PECVD). This structure was designed to maximize both device performance and manufacturing production throughput [23].

In this study, we compare the impact of different BCE etchants on the characteristics of the inverted staggered advanced a-Si:H TFT, and identify a promising dry etchant that is capable of producing transistors with comparable electrical performance as the device etched by a wet etchant.

2. a-Si:H TFT fabrication

We fabricated inverted staggered amorphous silicon thin-film transistors (a-Si:H TFT) by sputtering 2000 Å of chromium, and using photolithography and wet etching (CR-14) to define the gate (#1), on oxidized silicon wafers (10 kÅ of thermal oxide). All the transistors have the same channel widths (121 μm) and channel lengths (103 μm). Afterward 3500 Å of high deposition rate a-SiN_X:H (G2), 500 Å of low deposition rate a-SiN_X:H (G1), 1400 Å of high deposition rate a-Si:H (A2), 300 Å of low deposition rate a-Si:H (A1), and 700 Å of n^+a-Si:H (phosphorous doped to 1%) are sequentially deposited using PECVD to form the dual-layer gate insulator, dual-layer active channel layer, and the source/drain (S/D) contact layers, respectively [23]. The total amorphous silicon thickness ($t_{a\text{-}Si:H}$) is 1700 Å. The active island (#2) and gate via (#3) are successfully defined and dry etched with $SF_6 + Cl_2 + O_2 + He$ (6:24:20:5) and $CF_4 + O_2$ (20:1), respectively. Next 2000 Å of molybdenum (Mo) is sputtered as the S/D metal. Photolithography and wet etching (Al Etch Type A) are used to define the source and drain electrode (#4). After the etching of the top metal electrodes, the positive tone photoresist layer (Shipley 1813) remains on the molybdenum source and drain electrodes as the mask for the back channel dry etch process (Fig. 1b). This PR layer is necessary to shield the molybdenum film from direct ion bombardment during the RIE in order to prevent top layer molybdenum consumption and the contamination of the TFT back channel due to metallic residue (e.g. MoF_X and/or $MoCl_X$) formation [22]. Four different etching chemistries, three dry and one wet, are used for the back channel etch (BCE) process of the advanced a-Si:H TFT (#5). Two of the dry-etch experiments, $HBr + Cl_2$ (1:1) and C_2F_6, are done in the LAM 9400 transformer-coupled plasma reactive ion etcher

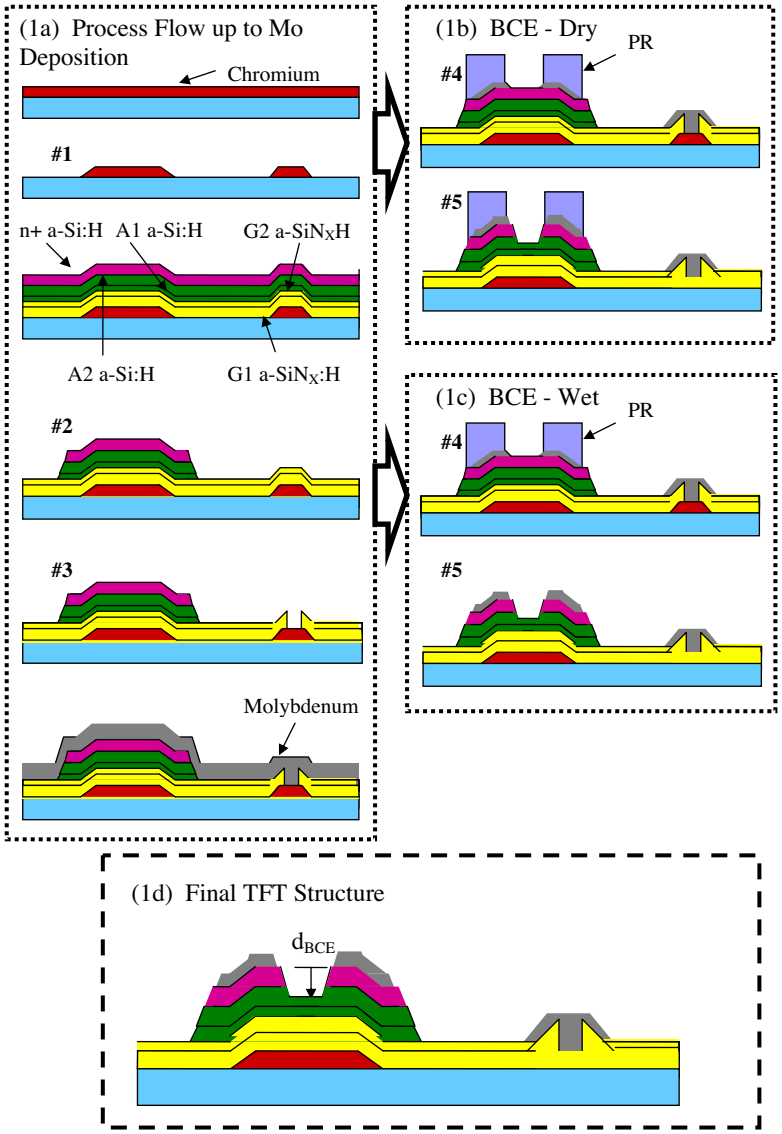

Fig. 1. Complete fabrication steps of the advanced a-Si:H transistor: (a) represents the fabrication process up to the source/drain molybdenum deposition, (b) shows the dry BCE process, with photoresist left on the source/drain as the etching mask, (c) shows the wet BCE process, which removes the PR during the back channel etch of the amorphous silicon film and (d) is the schematic of the final a-Si:H TFT structure.

Table 1
Etching chemistry and conditions for back channel etch process used in this study, and their respective etch rates for PECVD a-Si:H and n$^+$a-Si:H films.

Etchant	TCP-RF (W)	Bias RF (W)	Pressure (mTorr)	a-Si:H/n$^+$a-Si:H etch rate (Å/min)
$HBr:Cl_2$ (1:1)	100	30	12	400/680
C_2F_6	200	80	12	310/350
$CCl_2F_2:O_2$ (5:1)	–	100	100	150/300
KOH	–	–	–	1200/1500
$SF_6:Cl_2:O_2$:He (6:20:20:5)	100	30	12	1280/1640

(TCP-RIE), and the third, $CCl_2F_2 + O_2$ (5:1), in a capacitive-coupled reactive ion etcher (Table 1). The wet etching of the amorphous silicon active layer is done in a 50 °C solution comprised of 400 g of potassium hydroxide (KOH) pellets dissolved in 4000 mL of deionized water; only molybdenum is used as the mask for the KOH etching because the alkali-based solution attacks positive tone PR (Fig. 1c). After the BCE and the removal of the photoresist, the TFTs are annealed in nitrogen for 1 h at 200 °C to remove plasma-induced radiation damages induced in the a-SiN:H and a-Si:H films [24]. Fig. 1 shows the fabrication steps used in this study. The fabricated devices were not passivated with any passivation layer. It should be mentioned here that we perform a 10% over-etch, by intentionally extending the etch time, during the gate and S/D metals etching steps, and the island etching step, to avoid unwanted electrical shorts between the device features. The TFT's electrical characteristics are measured and extracted using methods described previously [23]. Table 1 shows the detailed etching recipes and etch rates of the four BCE etchants used for the etching of the a-Si:H and n$^+$a-Si:H films.

To investigate the effect of BCE etchants on the transistor performance, we first need to identify the best BCE etching depth (d_{BCE}) of the a-Si:H TFT for each etchant. Test wafers with the identical films and patterns, up to S/D electrode wet etch, undergo BCE using a specific etchant for a set duration. The final a-Si:H thicknesses ($d_{a\text{-}Si:H}$) is defined as $t_{a\text{-}Si:H}$–d_{BCE}, which is the a-Si:H thickness in the TFT's channel region. For TFTs etched with HBr + Cl_2, $d_{a\text{-}Si:H}$ values range from 1190 to 800 Å, and no over-etch time is included. Similar experiments are conducted using other etchants for the back channel etch process. The electrical characteristics of the best transistor for each etchant will be used as the basis of comparison regarding the impact of BCE etchant chemistry and discussion of its mechanism.

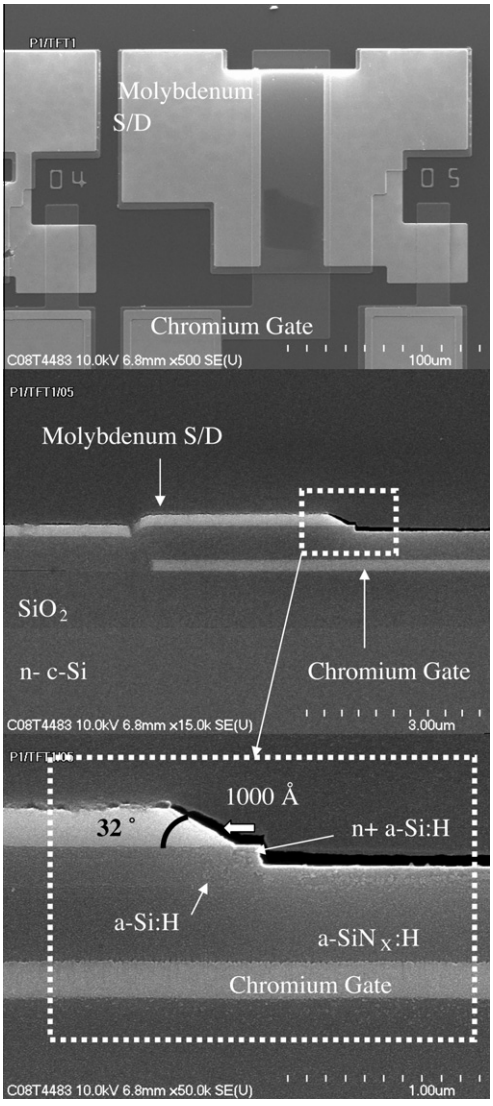

Fig. 2. SEM images of the a-Si:H TFT used in this work. The top image is the SEM top-view of the TFT (W/L = 121/43). The middle image shows the cross-sectional SEM image of the a-Si:H TFT, and the bottom SEM image shows detailed etching profile of the TFT near the source electrode.

3. Results and discussion

3.1. Impact of the gate and source/drain metal wet etch

We show in Fig. 2 the scanning electron microscope images of the S/D region of the inverted staggered a-Si:H TFT fabricated in this work. Wet etchant was used for the S/D electrodes fabrication, and we notice that the molybdenum electrode is over-etched by about 1000 Å, which is much larger than the initially targeted 10% over-etch, or 200 Å for the metal film. It is possible that the lateral etch is faster than the vertical etch due to the stress of the film. Among the three etched layers (gate, S/D, and n$^+$a-Si:H/a-Si:H), only the molybdenum S/D shows tapered profile, with a tapered angle of about 32° as measured from the surface of the film. Such low tapered angle for the film is achieved by using wet etchant that is highly isotropic (i.e. significant lateral etching underneath the photoresist mask occurs). This high lateral etch rate can also explain the excessive molybdenum S/D over-etch mentioned above.

A low tapered angle is a very desirable property since it can improve the overall active-matrix liquid crystal displays (AM-LCD) production yield. During the fabrication of AM-LCD panels, there are multiple levels of film deposition and etching steps that are required to produce fully functional products [25]. Each thin-film's contour and conformity is influenced by the surface morphology of the underlying layers [26]. In the case of the a-Si:H TFT presented in this work, the gate metal and n$^+$a-Si:H etchings produce sharp corners (i.e. large tapered angle) near their respective edges; the sharp corners can reduce the step coverage of the films deposited afterward (e.g. molybdenum). Such contact profile near the electrode corner can be highly strained, and lead to the delamination and/or buckling of the subsequent film. If a strain-induced fissure is created in a metallic film, it can potentially create unwanted open circuits, leading to a failure in the electronic operation. For the traditional AM-LCD fabrication process [25], the films deposited after the molybdenum (data) lines are the passivation amorphous silicon nitride, and the ITO pixel electrode. Tapered data lines reduce the chance of unwanted open circuit connection between the data lines and the pixel electrodes, and increase the overall production yield. To further improve our a-Si:H TFT fabrication process, the etchants for the gate and n$^+$a-Si:H/a-Si:H should both be highly isotropic, so the data lines and the pixel electrodes can have better step coverage.

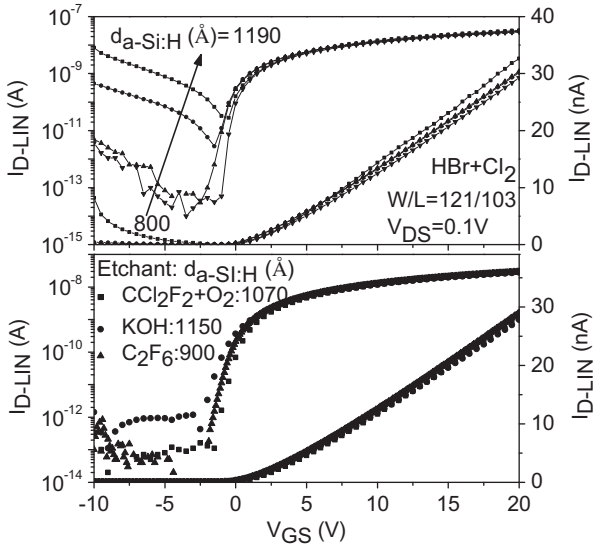

Fig. 3. Linear regime (V_{DS} = 0.1 V) transfer characteristics of a-Si:H TFTs etched with HBr + Cl_2 (top) for different $d_{a\text{-}Si:H}$, and CCl_2F_2 + O_2, C_2F_6, and KOH (bottom).

3.2. Impact of the amorphous silicon film thickness within the TFT channel

Figs. 3 (top) and 4 (top) show the linear and saturation regime characteristics for advanced a-Si:H TFT's etched with the HBr recipe during the BCE process for different $d_{a\text{-}Si:H}$ values. Based on these characteristics we extract the transistors' electrical parameters as shown as an example in Fig. 5. The summary of the average of three measurements is shown in Fig. 6 by plotting them against $d_{a\text{-}Si:H}$. The a-Si:H TFT's off current and subthreshold swing (S) both decrease with decreasing $d_{a\text{-}Si:H}$. The transistors' field-effect mobility shows a 9% decrease as $d_{a\text{-}Si:H}$ changes from 1190 to 1070 Å, and remains constant as the $d_{a\text{-}Si:H}$ decreases down to 800 Å; the threshold voltage values appear to increase as $d_{a\text{-}Si:H}$ decreases. However, since μ_{EFF} and V_T error bars are about ±0.07 $cm^2\ V^{-1}\ s^{-1}$ and ±0.23 V, respectively, the changes are accounted as statistical fluctuation, which means both parameters remain unchanged with $d_{a\text{-}Si:H}$. Since all of the a-Si:H TFT's have identical initial a-Si:H film

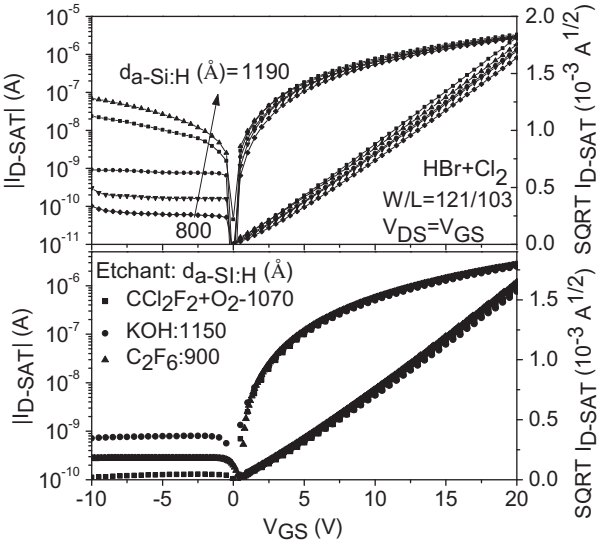

Fig. 4. Saturation regime ($V_{DS} = V_{GS}$) transfer characteristics of a-Si:H TFTs etched with HBr + Cl_2 (top) for different $d_{a\text{-}Si:H}$, and CCl_2F_2 + O_2, C_2F_6, and KOH (bottom).

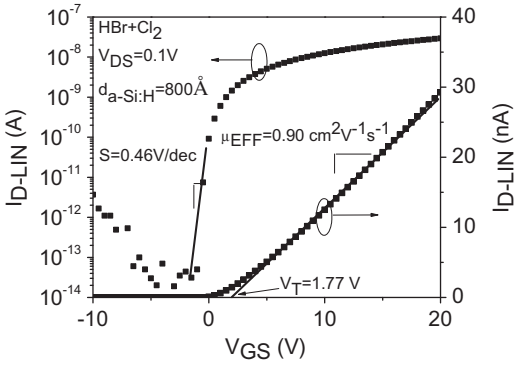

Fig. 5. Example of a-Si:H TFT electrical characteristics extraction. The device shown is etched with HBr + Cl_2 and the $d_{a\text{-}Si:H}$ value is 800 Å.

thickness values (prior to the BCE), and the device structure is an inverted staggered TFT, we do not expect any difference in the electronic qualities of the a-Si:H film, front interface qualities, nor the transistors' S/D contact resistances. Both TFT μ_{EFF} and V_T values remain constant, within statistical range, as $d_{a\text{-}Si:H}$ decreases from 1190 to 800 Å. This observation, together with the fact that all transistors have similar electrical and geometric parameters other than $d_{a\text{-}Si:H}$, leads us to conclude that the channel region a-Si:H film thickness after BCE does not impact the TFT's field-effect mobility and threshold voltage.

The drastic reduction ($\sim 10^4$) in a-Si:H TFT I_{OFF} with the thinning $d_{a\text{-}Si:H}$ can be explained by the removal of the phosphorous doped a-Si:H film in the back channel (a-Si:H/atmosphere interface), which causes a leakage path between the source and the drain of the a-Si:H TFT [12]. During the sequential PECVD deposition of the a-SiN_X:H, a-Si:H, and n^+a-Si:H, phosphorous atoms in the n^+a-Si:H layer diffuse in the neighboring a-Si:H film for an additional few 100's Å. The activation of these dopants in the a-Si:H leads to the increasing conductivity of the film due to higher electron concentration. Since the Fermi-level in the back interface of a-Si:H is much closer to the conduction band then in the a-Si:H bulk, negative voltage applied to the gate of the transistor is insufficient to "turn-off" the electrical current conduction path in the back channel. Thus electrons can conduct between the source and drain of the TFT along the phosphorous-rich a-Si:H film near the back channel when $d_{a\text{-}Si:H}$ is thick. As the back channel of the a-Si:H film is gradually etched away, the highly conductive section of the film disappears and the off-current is reduced.

The most puzzling trend is observed in the subthreshold swing: S decreases with decreasing $d_{a\text{-}Si:H}$. It is well known that the generation of deep-gap and interface states causes S to increase [23,27]. As $d_{a\text{-}Si:H}$ decreases, it is unlikely that the densities of states (DOS) of the bulk amorphous silicon film, and the front (a-SiN_X:H/a-Si:H) and back interfaces improve. Moreover, it has been shown that there is a linear correlation between S and V_T [28], which we do not observe. We believe that the observed higher S values of TFT's with thicker $d_{a\text{-}Si:H}$ (i.e. 1190 and 1070 Å) is related to a high I_{OFF} originating from the back channel conduction. In these devices a significant portion of the electrical conduction occurs in the back channel of the a-Si:H TFT. These electrons flow in the a-Si:H film (A2) with a higher bulk deep-gap state density [24] compared to the a-Si:H film (A1) in the front channel. Furthermore, I_{OFF} also flows near the back interface, which has a higher surface deep-gap state density then the front interface due to less ideal deposition conditions [24]. Higher deep-gap state densities at both locations can lead to the higher S values, because the Fermi-level near the back interface gets pinned in those transistors [10]. This explains why transistors with thicker $d_{a\text{-}Si:H}$ shows a higher S. These higher extracted subthreshold swings account for both front

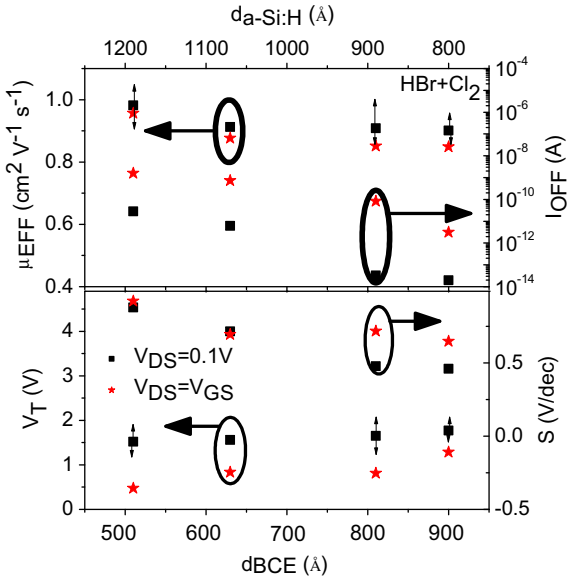

Fig. 6. Amorphous silicon TFTs' field-effect mobility, threshold voltage, subthreshold swing, and off current values change with $d_{a\text{-}Si:H}$. All transistors are etched using HBr + Cl_2.

and back channel conduction behaviors. Once $d_{a\text{-}Si:H}$ becomes thinner (i.e. 890 and 800 Å), I_{OFF} decreases due to the reduced phosphorous concentration in the back channel, and consequently, the subthreshold swing values decreases. For such device, a large number of electrons begin to flow in A1 a-Si:H with lower DOS. This trend does not imply that the front channel a-Si:H bulk and interface DOS improves with the progressive etching of $d_{a\text{-}Si:H}$, but rather the contribution of the back channel decreases with the reduction of $d_{a\text{-}Si:H}$.

In summary, about 800 Å of amorphous silicon film was etched away during the BCE process to achieve an acceptably low I_{OFF} ($\sim 10^{-14}$ A) for a-Si:H TFT. We do not observe any changes in μ_{EFF}, V_T, and S as $d_{a\text{-}Si:H}$ decreases from 1190 to 800 Å. Advanced a-Si:H TFTs show adequate electrical performance with 800 Å, 300 Å of A1 and 500 Å of A2, of amorphous silicon film remained in the active channel region. For the fabrication of inverted staggered BCE type advanced a-Si:H TFT, we recommend the a-Si:H film deposition thickness to be at least 1600 Å to realize transistors with reasonably low I_{OFF} and high electrical performance.

3.3. Impact of the back channel etchant chemistry

Our next experiment will assess the impact of BCE etchants on the electrical performance of the advanced a-Si:H TFT's. Three of the four etchants expose transistors to plasma and radiations, with KOH being the only one that relies purely on the chemical reaction to etch the n^+a-Si:H films; the chemical reaction of the KOH etching of silicon can be described by [29]:

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2. \quad (1)$$

Although the three dry etch recipes are all carried out in plasma chambers, their silicon etching mechanisms are quite different. CCl_2F_2 molecule contains both fluorine and chlorine atoms, yet the primary species involved in the etching of amorphous silicon is chlorine [30]. The reason for this is that the C–F bond is stronger then the C–Cl bond, and in CCl_2F_2 there is a higher probability to remove the chlorine atoms from the molecule [30]. Gerlach-Meyer et al. have demonstrated that chlorine atoms require ion bombardment to chemically react with silicon atoms, and that the volatile etching product formed is $SiCl_4$ [31]. Other etching products can also be formed following the chemical reaction between chlorine and silicon: SiCl, $SiCl_2$, and $SiCl_4$ [32]. For the HBr + Cl_2 chemistry, both bromine and chlorine ions participate in the etching of silicon. Similar to the chlorine etching of silicon, in order to achieve an effective HBr etching of the amorphous silicon, it is important to bombard the silicon with ionized bromine to overcome the activation energy necessary to trigger the chemical reaction between the bromine and the silicon atoms. As a result, using HBr + Cl_2 chemistry as the back channel etchant should lead to highly anisotropic n^+profile, which can be seen in the SEM images in Fig. 2. The volatile product formed is $SiBr_4$ [33]:

$$Si + 4HBr \rightarrow SiBr_4 + 2H_2. \quad (2)$$

Other non-volatile etching by-product ($SiBr_X$) can also be formed and deposited on the sidewall [34]. Unlike the two dry etching recipes mentioned, C_2F_6 etching involves the chemical interaction between the fluorine and the silicon atoms. Since the activation energy required is quite low (0.1 eV), fluorine-based dry etching of silicon can be triggered with little or no ion bombardment [32]. Among the three dry etching chemistry used in this study, $CCl_2F_2 + O_2$ and HBr + Cl_2 require more physical ion bombardment to activate the etching process. This means that they tend to produce higher anisotropy of the profile. C_2F_6 on the other hand, relies heavily on the chemical reaction to etch silicon, which indicates that it produces more isotropic etching profiles.

Figs. 3 (bottom) and 4 (bottom) show the transfer characteristics of the advanced a-Si:H TFT's fabricated with four different BCE etchant chemistries. The summary of their electrical parameters in the linear region of operation is shown in Fig. 7; the saturation region of operation parameters are similar in values and trends and will not be shown here. These data represent the electrical characteristics of the a-Si:H TFT's with optimized $d_{a\text{-}Si:H}$ (Å): HBr + Cl_2 (800), $CCl_2F_2 + O_2$ (1070), C_2F_6 (900), and KOH (1150). The TFTs' field-effect mobility, threshold voltage, and subthreshold swing values show no change when different BCE etchants are used. This consistency among the extracted electrical parameters suggests that the density of states in the amorphous silicon film and the front channel interface do not change during the back channel etching process. I_{OFF} for the dry-etched a-Si:H TFT's have similar values, but the KOH etched TFT has approximately one order of magnitude higher off current value. This is due to a layer of conductive alkali residue left in the back channel of the TFT during the KOH etching of the amorphous silicon film [18]. According to our experiment, the presence of plasma does not significantly or permanently degrade the electrical performance of the advanced a-Si:H TFT since their μ_{EFF}, V_T, and S have very similar values. HBr + Cl_2 chemistry can be used for the BCE step because we observe no electrical degradation caused by plasma and radiation, and it offers excellent selectivity over a-SiN_X:H (>200:1).

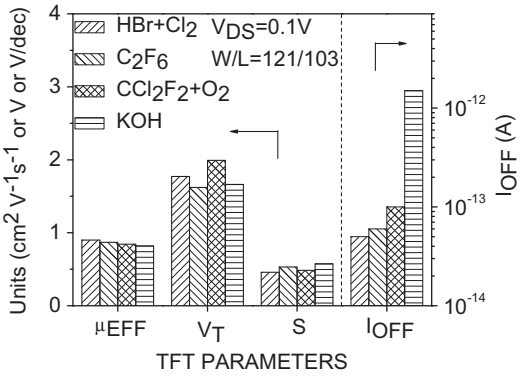

Fig. 7. Optimum a-Si:H TFTs' field-effect mobility, threshold voltage, subthreshold swing, and off current values comparison.

4. Conclusion

Based on our experimental results, the deposition thickness of a-Si:H film for advanced a-Si:H TFT should be at least 1600 Å. This allows the etching of the back channel a-Si:H film (~800 Å) for the purpose of reducing I_{OFF} without degrading, caused by an over-etching of the a-Si:H, the electrical properties of the transistor. We have shown that by utilizing RIE for the BCE process, we can obtain transistors with similar electrical characteristics as those etched with the KOH. There seems to be no significant correlation between the dry etch chemistry and the transistors' device performance for the investigated etching chemistries in this work. We recommend using HBr + Cl_2 as the etchant gas for the BCE process because of its acceptable n^+a-Si:H and a-Si:H etch rates and selectivity (1.7:1), and excellent a-Si:H/a-SiN_X selectivity (>200:1). Further research should be done to obtain a tapered etching profile during the BCE process for the fabrication of commercial AM-LCD.

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